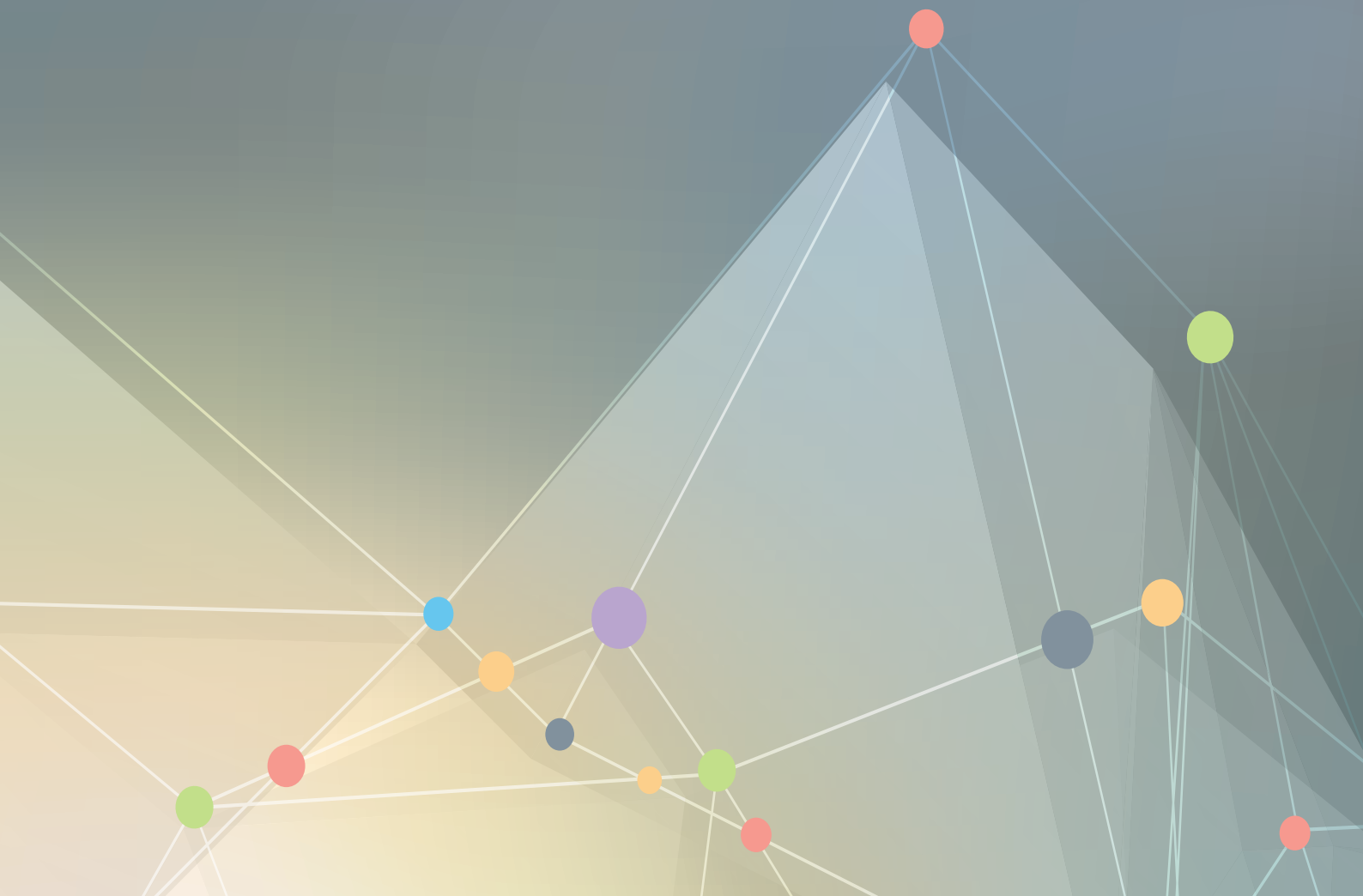
BOOK OF ABSTRACTS

Oral Presentations



C'Nano
THE NANOSCIENCE MEETING
2023

Poitiers
March, 15, 16 and 17

Nano-electronics

(Last update: November 2nd, 2022)

Description

This session is open to basic, applied and technological research. It will cover recent developments in nanoelectronics, including high frequency and power electronics, new calculation paradigms, and emerging types of memories .
This session will particularly focus on:

- High frequency switches, radio-frequency devices and THz applications
- Advanced device fabrication and new architecture paradigms such as Neuromorphic computing
- Memory and spintronics
- High power electronics and AC/DC conversion
- New materials including 2D materials such as graphene and transition metal dichalcogenide layers.
- Superconducting qubits

Keywords

Power RF and THz electronics, memory, bio-inspired-computing, 2D materials, qubits

Scientific committee

Anthony AYARI* (CNRS – ILM, Villeurbanne)
Matthieu JAMET (CEA–SPINTEC, Grenoble)
Philippe BOUCAUD* (CNRS – CRHEA, Sophia Antipolis)
** Session Coordinator*

In partnership with PEPR electronics

Wednesday March 15th

3.30 pm – 6.00pm

Room 13/14

Program of the session

Chairs: Philippe BOUCAUD & Matthieu JAMET

NANOELECTRONICS		
15:30	**Enabling full fault tolerant quantum computing with silicon based VLSI technologies**	**Maud VINET** • *SiQuance, Grenoble – France)*
16:00	Leveraging Physics for Energy-Efficient Artificial Intelligence	**Damien QUERLIOZ*** • *CNRS - C2N, France*
16:45	Coffee & tea break	
17:15	Localised growth of Vertical GaN devices on large diameter silicon substrates	**Matthew CHARLES*** • *CEA - LETI, France*
17:45	Large Scale Integration of 2D material for RF switches	**Clotilde LIGAUD*** • *CEA - LETI, France*

* Invited speakers

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Maud VINET

Siquance I Chief executive officer & Researcher

Electronics and Information Technology Laboratory

www.siquance.com

Biography

Maud VINET is currently CEO of Siquance, as start-up company aiming at developing and commercializing a quantum computer based on silicon.
She was previously leading the quantum computing program in Leti. Together with Tristan Meunier (CNRS) and Silvano de Franceschi (Fundamental research division from CEA), they received an ERC Synergy grant in 2018 to develop silicon based quantum computer.
She defended a PhD of Physics from University of Grenoble Alps and was hired Leti in 2001 as a CMOS integration and device engineer. From 2009 to 2013, she spent 4 years in Albany (NY, US) to develop Fully Depleted SOI within IBM Alliance together with STMicroelectronics. In 2015, she spent 6 month with Globalfoundries in Malta, NY to launch 22FDX program. From 2013 to 2018, she managed the Advanced CMOS integration team activities in Leti.
Maud Vinet authored or co-authored about 300 papers, she owns more than 70 patents related to nanotechnology and her Google h-index is 52 with more than 11000 citations.

Enabling full fault tolerant quantum computing with silicon based VLSI technologies

Quantum computing when available will tackle life changing applications, like in energy or chemistry. Silicon has the ability to enable this full quantum advantage leveraging Very-Large-Scale Integration (VLSI) fabrication and design techniques. First scientific demonstrations have been made, it's now up to electrical engineers in collaboration with physicist to turn these demonstrations into practical machines.

Keywords:

Quantum computing; semiconductor; CMOS technology

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The comment was requested by Nature Nanotechnol. editors to share on the prospects for semiconductor/spin qubit-based quantum computing in particular in the technology angle, i.e., scalability, compatibility with standard CMOS tech etc.
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Scaling silicon-based quantum computing using CMOS technology.
Nat Electron 4, 872–884 (2021). https://doi.org/10.1038/s41928-021-00681-y
This review paper was requested by Nature Electronics editors and reviews some technological challenges of spin qubits.

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Keywords: memristors, in-memory computing, energy-efficient AI, Bayesian nanoelectronics
Disciplinary fields involved: Electrical Engineering, Physics, Artificial Intelligence
Sustainable Development Goals: Good Health and Well-being (Goal 3), Sustainable Cities and Communities (Goal 11)

Leveraging Physics for Energy-Efficient Artificial Intelligence

Damien Querlioz

Université Paris-Saclay, CNRS, Centre de Nanosciences et de Nanotechnologies, Palaiseau, France.

The field of artificial intelligence (AI) has seen rapid advancements in recent years, but with it comes an unsustainable energy cost. Training modern AI models requires gigawatt-hours of electricity, largely due to the inefficiency of moving data between logic and memory units in traditional computers. In contrast, brains achieve superior energy efficiency by seamlessly integrating logic and memory in an "in-memory" computing style. However, achieving this type of integration at large scale using traditional electronics technology has been a significant challenge. Recent developments in memory devices that employ new physics principles, such as memristive, phase change, and magnetic memories, have opened the door to achieving an extremely tight integration between logic and memory. However, these devices also come with their own set of challenges due to their unreliable nature, which originates from their underlying physics. In this talk, we will explore how inspiration from neuroscience can be used to extract lessons on the design of in-memory computing systems, exploiting the physics of unreliable devices. We will study the reliance of brains on approximate memory strategies and how they can be replicated for machine learning. We will present the example of a memristor-based Bayesian machine, which recognizes human gestures using thousands of times less energy than a competing microcontroller unit. Additionally, we will present a second approach where the probabilistic nature of emerging memories is fully exploited for probabilistic learning. We will demonstrate how an array of 16,384 memristors can be trained to recognize images of cancerous tissues using this technique. Finally, we will discuss the prospects for implementing various learning algorithms with emerging memories.

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Keywords: GaN-on-silicon, vertical devices, localized growth
Disciplinary fields involved: Physics, materials science
Sustainable Development Goals* eventually involved in your research: Affordable and clean energy (Goal 7); Climate action (Goal 13)

Localised Growth of Vertical GaN devices on large diameter silicon substrates

Matthew Charles[1]

1. *Univ. Grenoble Alpes, CEA, LETI, 38000 Grenoble, France*

For future energy needs, more and more of the economy will be powered by electricity, in particular renewable energy. In order to facilitate this evolution, conversion losses must be reduced, in order to efficiently use the electricity generated.
Currently silicon is still the most common material used for power electronics convertors, but wide bandgap materials such as silicon carbide (SiC) or gallium nitride (GaN) offer possibilities for big reductions in losses. SiC wafers are available in large diameter, but are still expensive, while GaN wafers are even more expensive and less mature. However, GaN has the advantage that it can be grown on non-native substrates such as silicon, bringing the enticing prospect of wide bandgap performance at silicon prices, and with silicon processing steps.
Currently GaN on silicon devices are lateral high electron mobility transistors (HEMTs) which are compatible with 650V devices. Higher voltages would be interesting for even more power applications, and verticalisation of devices would lead to smaller surface area devices, and so lower costs. However, to grow the necessary 10 µm of GaN required for these devices on silicon is extremely challenging. At LETI, we are developing localized growth of GaN on silicon and this presentation will show the latest developments to achieve the material specifications required, with thick layers, uniform island growth, and low un-intentional doping levels.

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Keywords: 2D material, Integration, RF switch
Disciplinary field involved: Physics

Large Scale Integration of 2D material for RF switches

Clotilde Ligaud[1], Pierre Trousset[1], Lucie Le Van-Jodin[1], Bruno Reig[1], Clémence Hellion[1], Paul Brunet[1], Céline Vergnaud[2], Hanako Okuno[2], Djordje Dosenovic[2], Matthieu Jamet[2]

1. *CEA-Leti, Univ. Grenoble Alpes, F-38000 Grenoble, France*
2. *CEA-Irig, Univ. Grenoble Alpes, F-38000 Grenoble, France*

2D materials are promising candidates for next generation devices. Especially, switching behavior [1] has been demonstrated with TMD like MoS_2, which allows the manufacturing of memristors [2] or high cut-off frequency RF switches [3]. Nevertheless, the high growth temperature of 2D material by physical or chemical methods prevents their direct integration in circuits. An intermediate transfer step from the growth substrate to the final substrate is necessary to achieve their large-scale integration. Today, most publications are based on individual devices with a great lack of reproducibility and statistics. Here, we report the successful large-scale integration of MoS_2 in memristors reaching the current state of the art.

In this work, planar bottom electrodes are patterned on a 200 mm wafer by standard process from microelectronics. About 250 dies of 1 cm^2 were thus obtained. A large-scale process flow is developed by transferring and patterning MoS_2 and top electrodes on the dies, vertical memories and RF switches are performed with the following structure: bottom electrode/2D material/top electrode. Morphological characterizations by SEM, AFM, Raman spectroscopy show the good quality of the fabrication process.

Memories and radio-frequency devices are characterized exhibiting a reproducible resistance-switching behavior. Several cycles (7) are observed on several devices. The I_{ON}/I_{OFF} ratio is around 10^4. RF performances are also highlighted a typical behavior of RF switches devices with OFF-state and ON-state.

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